ABSTRACT

A method of forming dual gate dielectric layers that is extendable to satisfying requirements for 50 nm and 70 nm technology nodes is described. A substrate is provided with STI regions that separate device areas. An interfacial layer and a high k dielectric layer are sequentially deposited on the substrate. The two layers are removed over one device area and an ultra thin silicon oxynitride layer with an EOT < 10 nm is grown on the exposed device area. The high k dielectric layer is annealed during growth of the SiON dielectric layer. The high k dielectric layer is formed from a metal oxide or its silicate or aluminate and enables a low power device to be fabricated with an EOT < 1.8 nm with a suppressed leakage current. The method is compatible with a dual or triple oxide thickness process when forming multiple gates.